

SYNCHRONIZING WIRELESS NETWORKS

Wireless broadband communication networks require precision synchronization and high performance crystal oscillators. Synchronization plays a vital role in ensuring that information transfer is performed with an acceptable level of bit error rate and that the carrier frequency is held stable.

Sophisticated encoding techniques

With the requirement of higher data rates in higher frequency bands comes the requirement on more sophisticated transmission techniques. Some of these techniques are very sensitive to carrier frequency offsets, which are mainly caused by the inherent instabilities of the carrier frequency oscillators in the transmitter and the receiver. These offsets must be very small compared to the subcarrier spacing.

The basic objective of wireless network synchronization is to limit the occurrence of slips, that is when the receiving equipment will drop or repeat an entire frame of data. Slips can occur for two basic reasons. The first is the lack of frequency synchronization among the clocks in the connection, resulting in different clock rates. The second is phase movement, either in the communication link (such as jitter and wander), or between the source and receive clock.

Wireless links are characterized by the geometric delay and variations due to atmospheric effects. These delay variations occur at a relatively slow rate and is often called “wander”. Jitter on the other hand, is delay variations occurring at a higher rate. The contribution to jitter is due to the signal-to-noise ratio obtainable at the receiving end of the link.

There would be not problem at all for the timing in a wireless network if all clocks and all delays were perfectly stable. Then the clocks would only need an initial adjustment so that all would run at the same rate and the network would operate forever without errors due to timing defaults. However, this is not the case. The methods used for correcting signal transition time variations are to 1) correct the rate of the clock or 2) correct the signal bit sequences by changing their delays.

Clock frequency control

For clock frequency control, the principle of master-slave architectures remains dominant and there are some good reasons for this. Existing and evolving high traffic volume networks are hierarchical. The current practice in network synchronization planning and design provides four hierarchical layers of minimum accuracy and worst-case slip rates. Levels 1 and 2 are operated under the responsibility of the high capacity trunk transmission systems. All clocks controlling switching gear are assigned to level 3 or lower. Customer premises equipment (CPE) and private networks are assigned to level 4. A most important feature of a level 3 (slave) node clock is the ability to operate in holdover mode in the

case of the interruption of the reference transmission link. The performance of a slave clock running in holdover mode can be characterized by two parameters the first being the residual frequency offset existing at the moment of switchover. The second parameter is the frequency drift constant of the free-running oscillator.

Wireless synchronization requirements

Important synchronization requirements in a wireless network that directly relate to the crystal oscillator components are; fewer calibrations, stability in hold-over mode, fast operation after power cut, optimized base-band filtering, minimized carrier frequency offsets, and more efficient use of space on printed circuit boards.

Fewer calibrations - Frequency re-calibration eases long-term stability requirements and synchronization component cost but brings high maintenance costs.

Stability in holdover mode – In the case of interruption of the reference transmission link, the equipment has to operate in holdover mode. There are two major contributions to holdover performance: initial frequency offset and frequency drift. Initial frequency offset is caused by the settability of the crystal oscillator frequency. Frequency drift occurs due to aging of the quartz crystal in the oscillator. Any frequency offset causes an accelerated phase drift proportional to the square of the running time. This effect will be dominant for longer holdover periods.

Stability in free-run mode – Customer premises Equipment (CPE) clocks are allowed to enter free-run mode when it loses all timing reference. Free-run mode refers to a mode of operation where the clock's timing is controlled by the local crystal oscillator and no memory of an external reference is used to correct the oscillator frequency. Operating in free-run mode poses large requirements on the overall stability of the local crystal oscillator.

Good long-term stability in the crystal oscillator minimizes the need for re-calibrations and enables stability in holdover and free-run mode operation. Long-term stability is one of the most challenging points in the crystal oscillator design. The effects of aging in the crystal resonator are reduced through extra care in the manufacturing process. Contamination control is one of the main issues in the production of high precision crystals. The process must clean the crystals all the way down to atomic level. A modern efficient process performs thorough cleaning of both surfaces of the crystal prior to electrode deposition by means of outgassing, UV-ozone cleaning (cracking) of adsorbed molecules, and atom bombardment.

Fast operation after power cut – If the power is cut, for example to perform maintenance, it is important that the equipment run at capacity in short time after power is turn on again. Superior retrace characteristics in the crystal oscillator shortens the time to operational capacity after a power cut. When an oscillator is turned off and then back on again, it will not usually resume at the same frequency at which it had been operating. Eventually, the oscillator will begin to age at its previous rate but will most likely be offset slightly from its original frequency. Retrace limits the accuracy achievable with oscillators in applications where it is on-off cycled. The mechanisms that can cause this effect include changes in the quartz resonator, resonator contamination, and oscillator electronics. These factors contributing to retrace effects are minimized by proper process control in the crystal production process. .

Optimized base band filtering – To minimize the risk that the desired signal is buried under the phase noise of adjacent strong channels, all jitter sources including the jitter contribution from the crystal oscillator must be minimized. In a typical wireless receiver, the local oscillator, usually implemented in a frequency synthesizer, provides the carrier signal necessary for the mixing process. The single-sideband (SSB) phase noise of the crystal oscillator is a critical performance parameter for the receiver. In phase-modulated digital communications systems such as Global System for Mobile Communications (GSM), the integrated phase noise of the synthesizer contributes to the RMS phase error of the transceiver. In a GSM receiver, when the Gaussian minimum-shift-keying (GMSK) signal is demodulated, the phase error will generate deviations in the location points within the demodulation's scheme constellation diagram. These deviations in the constellation points, which can be directly correlated to the crystal oscillator's phase noise, contribute to an increase in the system's bit-error-rate (BER). Given the impact of the crystal oscillators phase noise in the receiver, it is critical to find out what level of this noise will meet the required receiver performance. Low phase noise and the resulting stability of the crystal oscillators ensure minimal effect on base-band filtering and minimize carrier frequency offset. The high stability of a crystal oscillator is attributable to the steepness of the phase slope at the frequency of oscillation. The phase slope is determined by the crystal's unloaded Q-value, which in its turn depends on the **quality of the crystal processing technique**.

Minimized carrier frequency offsets – Some coding techniques are extremely sensitive to carrier frequency offsets, which are mainly caused by the inherent instabilities of the carrier frequency oscillators in the transmitter and receiver. These offsets must be very small compared to the subcarrier spacing.

Efficient use of space on printed circuit boards - The miniaturization of wireless infrastructure equipment creates a demand for surface mounted synchronization components with low height so that

they fit easily into a rack system. The power of high-performance crystal oscillators for the wireless market is the ability to combine small size with excellent performance.

Synchronization planning and high-performance crystal oscillators

The major contributor to synchronization performance in a wireless network operation is the frequency offset that a receiver clock exhibits relative to the primary reference source to which it is locked. This performance degradation can be controlled by proper synchronization planning and by the use of high-performance crystal oscillators. High-performance crystal frequency sources used in oscillators require a revolution in process technology. The difference can be recognized in the different factors in the crystal itself that affect frequency stability and therefore the quality of the entire wireless system. True modern crystal processing minimizes factors contributing to frequency instability, exhibits high yield, and is able to produce large volumes in short time. All this is necessary to meet the tough demands on performance and volumes posed by the wireless communications industry.